REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claims 6, 19 and 32 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 7, 13, 14, 20, 26, 27, 33 and 39 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Collodi. Claims 4, 5, 17, 18, 30 and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Collodi. The Collodi reference appears to be directed to a hardware extension to a programmable per-pixel shading device using a separate lighting sequence unit. Collodi describes a DX8 general purpose unit to which he adds a high precision lighting computation unit. As such, Collodi requires a fixed function lighting sequence unit. Applicants' claimed unified shader need not employ a separate fixed function lighting sequence unit as described in Collodi. Other differences will be apparent to those of ordinary skill in the art.

Since Collodi has been cited as anticipating claims 1, 7, 13, 14, 20, 26, 27, 33 and 39, it must contain all of the claimed subject matter. Applicants respectfully submit that Collodi fails to describe a unified shader as claimed that, among other things, has an input interface for receiving a packet from a rasterizer. Applicants are unable to find mention of packet information coming from a rasterizer as noted in the claim. As such, the claim is in condition for allowance. In addition, claim 1 requires for example, a unified shader comprising a "shading processing mechanism configured to produce a resultant value from said packet by performing one or more shading operations wherein the shading operations comprise both texture operations and color operations". As such, both color operations and texture operations are handled by the shading processing mechanism. The office action cites paragraphs 12 and 15 as allegedly teaching that the shaders in Collodi perform color

operations by determining "interpolated vertex color values". However, as described by Collodi, the "interpolated vertex color values" in paragraphs 12 and 15 are actually interpolated by the rasterizer 6 and not programmable shading unit 2 as alleged in the office action. Accordingly, the cited reference does not teach what is alleged and therefore the claims are in condition for allowance. Other differences will be recognized by one of ordinary skill in the art.

As to claims 4, 5, 17, 18, 30 and 31, the office action admits that Collodi fails to teach or suggest, among other things, a code partition mechanism to partition code configured to instruct the shading processing mechanism as claimed. However, the office action appears to merely make a conclusory statement that "coding refers to executable machine, which is the instruction of a program that was converted from source code to instruction so that the computer can understand." (Page 3 of office action). However, it is respectfully noted that this statement appears to misstate the claim language as the claim requires a code partition mechanism to partition code that has been configured to instruct the shading processing mechanism. The claim is not referring to merely coding as alleged in the office action. Accordingly, Applicants respectfully submit that the rejection does not provide a prima facie showing and that the claims are in condition for allowance as Collodi does not teach the claimed subject matter.

In addition, as noted in Applicants' Specification, code partitioning can help ensure that all ALUs and texture instructions pertaining to a given level of indirection are grouped together. As such, texture operations within the same level may effectively be executed in parallel. Such shader code partitioning is not taught or suggested by the cited reference.

In addition, the dependent claims add additional novel and non-obvious subject matter. For example, claim 5 requires that the partitioning mechanism groups code together by level of indirection. The office action does not address this claim language nor claim

language of other dependent claims. In any event, such operations are not taught or suggested by the cited art and accordingly, Applicants respectfully submit that the claim is in condition for allowance.

Claims 2, 3, 8-12, 15, 16, 21-25, 28, 29 and 34-38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Collodi in view of Zatz. As per claims 8-12, 21-25 and 34-38, it is alleged that Zatz teaches a plurality of ALU/memory pairs as claimed to perform shading operations.

The Zatz reference is directed to a method and apparatus for modifying depth values using pixel programs wherein depth values are calculated under control of pixel program using a variety of sources as inputs to programmable computation units in a programmable graphics system. The programmable computation units are used to compute traditional interpolated depth values and modified depth values. Zatz is alleged to teach the subject matter of claims 8-12, 21-25 and 34-38. However, the cited portion of Zatz namely column 2, lines 38-40 indicates that one or more arithmetic units are configured to compute an interpolated pixel depth value associated with its geometry primitive pixel and the cite to column 5 indicates that the shader core 330 outputs pixel data to a core backend FIFO. Applicants respectfully submit that the rejection does not address specific claim language in the claims. For example, claim 8 requires that the shader include ALU/memory pairs. However the cited portion in column 2, lines 38-40 does not teach such subject matter. In addition, claim 9 requires for example, that a plurality of ALU/memory pairs are synchronized by a scheduling clock mechanism. There is no such teaching or suggestion in the cited portions of any ALU/memory pairs with a scheduling mechanism. Similarly, the other dependent claims add additional novel and non-obvious subject matter. For example, claim 12 requires that the FIFO that does not have an associated buffer also comprise both data and operation instructions. However, the FIFO cited in the cited reference stores pixel

data as set forth in the cited portion and not operation instructions. Accordingly, this claim is also believed to be in condition for allowance. The other corresponding claims are also believed to be in condition for allowance for the same reasons.

Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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